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Will Release The Local Bus During T4 Of The Cycle When All The Following Conditions Are Met: 1.Request Occurs On Or Before T2. 2.Current Cycle Is Not The Low Byte Of A Word (on An Odd Address). 3.Current Cycle Is Not The First Acknowledge Of An Interrupt Acknowledge Sequence. 4.A Locked Instruction Is Not Currently Executing. Jun 4th, 2024

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Microprocessor Architecture Programming And
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Pearson, May 4th, 2024

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“Microcomputer Systems: The 8086 / 8088 Family -
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Edition, Prentice Hall Of India, 2007. 2. Mohamed Ali
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8086 Microprocessor (cont..) M. Krishna Kumar

MM/M1/LU3/V1/2004 2 • It Requires Single Phase Clock With 33% Duty Cycle To Provide Internal Timing. • 8086 Is Designed To Operate In Two Modes, Minimum And Maximum. • 1 May 2th, 2024

UNIT III 8086 MICROPROCESSOR INTERFACING

3.1 ...

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