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Condition Mainly Used With Binary Logic Elements Where The Logic State 1 (TRUE) Is Converted To A Logic State 0 (FALSE) Or Vice Versa [IEC 60617-12, IEC 61082-2] 3.20 Logic Inversion Condition Mainly Used With Binary Logic Elements Where A Higher Physical Level Is Converted To A Lower Physical Level Or Vice Versa [Feb 2th, 2024

#### **Using Image As Cipher Key In AES**

The Affine Transformation Element Of The S-Box Can Be Expressed As: Figure 4: Step 2 In S-Box Generation In AES 5.2 – Second Step: In This Step, Rows Swapped With Columns Of Primary S-Box In GenerateDynamicSbox(cipherKey) Function. This Function Guarantees New S-Box Remain One-for-one. This Routin Get Cipher Key As Input And Jan 24th, 2024

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