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2.5(RR) 2.5(R)(1arm&LHF) 1.5S No Arm 2.5S No Arm 3(RR) 3(R) ...

DESIGN: (Kato)HO2B P1 Armchair 1S 1arm(LHF) 1.5S
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1 Arm J1:1 - A518 (W) T Arm J1:2 - A518 (E) -

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1) 1 2 B B 1 T) 1 T 1 T 1 A B C. Full Input Data And
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And Compresses Data, Then Sends It Down A Channel
With Two Other Streams Of User Data, Each In Its Own
Time Slot. It O Jan 13th, 2024

ROBOTIC ARM CONTROL THROUGH HUMAN ARM

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Fig8. Screenshot Of AVR Studio 4 Running On Windows
7 Platform 21 Fig9. Screenshot Of SinaProg 2.0
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- V8 Simplified The Exception Model Vs V7? State, Privilege, Security Level Confusing Several Usr, Irq, Fiq, Svc, Und, Sys (also Hyp, Mon) - O Each Had It's Own Stack, Banked Registers And Briefly Used O Also Instruction State (J,T) -ARMv8 Only Arm64 Privilege -scattered Over Various States -usr-0, System -to Run Privileged Threads Apr 18th, 2024

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0 5 10 15 20 25 30 35 40 1 2 4 MIPS Number Of Cores (Instruction Set Simulators) Avg. ISS MIPS Acc. System MIPS 3 VP Simulation Performance N Example: UC/MC VP Performance (MIPS)-Target SW: COREMARK/Linux-Test Single/dual/quad Core Systems-In-house Instruction Set Simulator (ISS)-OSCI/Accellera1SystemC KernelReduced Simulation May 8th, 2024

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