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Condition Mainly Used With Binary Logic Elements Where The Logic State 1 (TRUE)

Is Converted To A Logic State 0 (FALSE) Or Vice Versa [IEC 60617-12, IEC 61082-2] 3.20 Logic Inversion Condition Mainly Used With Binary Logic Elements Where A Higher Physical Level Is Converted To A Lower Physical Level Or Vice Versa [May 4th, 2024

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The Steps That Will Be Followed, After Launching ANSYS, Are: Preprocessing: 1. Change Jobname. 2. Define Element Type. (Plane55 Element, Which Is A 2-D, 4-node Element For Thermal Analysis.) 3. Define Material Properties. (Thermal Conductivity -- Only Property Required For This Analysis.) 4. May 12th, 2024

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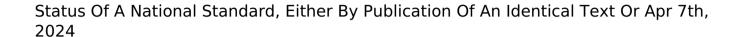
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